AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing Of Claims:

1. (Currently Amended) A wireless and passive tableting apparatus for computer inputting comprising a tablet and a pen, characterized in that

nothing wires the pen and the tablet and no battery is in the pen;

the tablet which can sense pressure from the pen comprises

a transmitting circuit comprising a plurality of coils in a first direction,

a receiving circuit comprising a plurality of coils in a second direction which is perpendicular to the first direction,

an amplifying circuit,

a phase angle and amplitude detecting circuit and

an integrating circuit; and

the pen comprises a parallel resonant circuit composed of capacitors and inductors;

the connection relations between them are as follows:

an auxiliary CPU, which generates a square wave continuously, connects with the transmitting circuit, which can transmit electromagnetic waves corresponding to the square wave continuously;

the pen circuit receives the electromagnetic wave transmitted from the transmitting circuit to produce and transmit a resonant signal;

the frequency of the resonant signal is different from the frequency of the transmitted electromagnetic waves;

the resonant signal is received by the receiving circuit continuously, and amplified by an amplifying circuit that connects with the receiving circuit;

the transmission of the electromagnetic waves and the receiving of the resonant signal occur simultaneously;

the amplified signals are inputted into the phase angle and amplitude detecting circuit, and

the signals output from the phase angle and amplitude detecting circuit are inputted into a primary CPU via the integrating circuit;

the connection relations of the amplifying circuit in the tablet are as follows:

a (RX+) terminal for receiving signals connects with ends of first and second parallel resistors (R1 and R2), the other end of the second resistor (R2) connects with a negative input pin (2) of a first amplifier (IC12A) and one end of a third resistor (R3) in parallel, and the other end of the third resistor (R3) connects with an output pin (1) of the first amplifier (IC12A), a first pin (12) of an amplifying circuit chip (IC14) and one end of a fourth resistor (R6);

a grounding pin (4) of the first amplifier (IC12A) is connected to analogue ground;

the other end of the first resistor (R1) connects with one end of a fifth resistor (R4), a first capacitor (C6) and a reference voltage terminal;

the other end of the fifth resistor (R4) connects with a positive input pin (3) of the first amplifier (IC12A), the other end of the first capacitor (C6) is connected to analogue ground and one end of a second capacitor (C7), the other end of the second capacitor (C7) connects with a power supply connection pin (8) of the first amplifier (IC12A) and a first power supply (VDD);

the other end of the fourth resistor (R6) connects with a second pin (13) of said chip (IC14) and one end of a sixth resistor (R7);

the other end of the sixth resistor (R7) connects with a third pin 14 of said chip (IC14) and one end of a seventh resistor (R8);

the other end of the seventh resistor (R8) connects with a fourth pin (15) of said chip (IC14) and one end of an eighth resistor (R9);

the other end of the eighth resistor (R9) connects with a fifth pin (1) of said chip (IC14) and one end of a ninth resistor (R10);

the other end of the ninth resistor (R10) connects with a sixth pin (2) of said chip (IC14) and one end of a tenth resistor (R11);

the other end of the tenth resistor (R11) connects with a seventh pin (4) of said chip (IC14) and one end of an eleventh resistor (R12);

the other end of the eleventh resistor (R12) connects with an eighth pin (5) of said chip (IC14) and one end of a twelfth resistor (R13);

the other end of the twelfth resistor (R13) connects with a reference voltage terminal;

a ninth pin (3) of said chip (IC14) connects with one end of a third capacitor (C1), the other end of the third capacitor (C1) connects with one end of a thirteenth resistor (R16) and a positive input pin (5) of a second amplifier (IC12B);

the other end of the thirteenth resistor (R16) connects with the reference voltage terminal;

an output pin (7) of the second amplifier IC12B, which outputs the output signals, connects with one end of a fourteenth resistor (R26);

the other end of the fourteenth resistor (R26) connects with a negative input pin (6) of the second amplifier (IC12B) and one end of a fifteenth resistor (R23);

the other end of the fifteenth resistor (R23) connects with the reference voltage terminal;

a tenth pin (11) of said chip (IC14) connects with a first signal connection (GA), and an eleventh pin (10) of said chip (IC14) connects with a second signal connection (GB) and a twelfth pin (9) of said chip (IC14) connects with a third signal connection (GC), and a thirteenth pin (16) of said chip (IC14) connects with the first power supply (VDD) and one end of a fourth capacitor (C14);

the other end of the fourth capacitor (C14) connects with the analogue ground, and a fourteenth pin (6), a fifteenth pin (7) and a sixteenth pin (8) of said chip (IC14) connect with analogue ground.

2. (Currently Amended) The wireless and passive tableting apparatus of claim 1, wherein

the transmitting circuit and receiving circuit comprise ~~coils in a first direction (Y), coils in a second direction (X) and~~ chips;

(RX+) terminals of the receiving circuit are connected to pins ~~(3)~~ corresponding to ports ~~(X)~~ of each of a set of chips (L10, L11, L12, L13, L14 and L15);

for a first subset of chips (L10, L11 and L12),

said chips have (X0-X7) ports corresponding to pins (13, 14, 15, 12, 1, 5, 2 and 4) connecting with the coils in the ~~first~~ second direction ~~(Y)~~ respectively,

the coils have output terminals which are grounded,

said chips have (INH) terminals corresponding to pins (6) used for chip selection,

said chips have terminals (A, B, C) corresponding to pins (11, 10 and 9) which are gating terminals, all connecting with the primary CPU, and

each of said chips has a (VEE) terminal corresponding to a pin (7) connected to a negative voltage;

the square wave generated by the auxiliary CPU is inputted into a pin ~~(3)~~ corresponding to a port ~~(X)~~ of each of a second subset of chips (L13, L14, and L15) via (TX+) terminals of the transmitting circuit; and

for the second subset of chips (L13, L14, and L15),

said chips have (X0-X7) ports corresponding to pins (13, 14, 15, 12, 1, 5, 2 and 4) connecting with the coils in the first direction ~~(Y)~~ respectively,

the coils have output terminals which are grounded,

said chips have (INH) terminals corresponding to pins (6) used for chip selection,

said chips have terminals (A, B, C) corresponding to pins (11, 10 and 9) which are gating terminals, all connecting with the primary CPU, and

each of said chips has a (VEE) terminal corresponding to a pin (7) connected to a negative voltage.

3. (Cancelled)

4. (Previously Presented) The wireless and passive tableting apparatus of claim 1, wherein, the connection relations of the phase angle and amplitude detecting circuit are as follows:

an input (IN) terminal connects with a positive input pin (3) of a third amplifier (IC9A) and one end of a sixteenth resistor (R17) in parallel, the other end of the sixteenth resistor (R17) connects with a negative input pin (6) of the fourth amplifier (IC9B) and one end of a seventeenth resistor (R18) in parallel, the other end of the seventeenth resistor (R18) connects with an output pin (7) of the fourth amplifier (IC9B) and a first connection pin (4) of a first detecting circuit chip (IC8B) in parallel;

a positive input pin (5) of the fourth amplifier (IC9B) connects with one end of an eighteenth resistor (R19), the other end of the eighteenth resistor (R19) connects with a reference voltage;

an output pin (1) of the third amplifier (IC9A) connects with a negative input pin (2) of the third amplifier (IC9A) and a first connection pin (8) of a second detecting circuit chip (IC8C);

a power supply connection pin (8) of the third amplifier (IC9A) is connected to a first power supply (VDD), and grounding pin (4) of the third amplifier (IC9A) connects with an analogue ground;

a second connection pin (5) of the first detecting circuit chip (IC8B) connects with a first pin (2) of an auxiliary CPU (MCU2);

a second connection pin (6) of the second detecting circuit chip (IC8C) connects with a second pin (3) of the auxiliary CPU (MCU2);

an output pin (3) of the first detecting circuit chip (IC8B) and an output pin (9) of the second detecting circuit chip (IC8C) are connected together, used as an output terminal;

a third pin (11) of the auxiliary CPU (MCU2) connects with ends of a fifth capacitor (C4) and a nineteenth resistor (R28) in parallel, wherein two other ends of the fifth capacitor (C4) and the nineteenth resistor (R28) are connected together to connect with a base of a triode (Q1), whose emitter connects with one end of a sixth capacitor (C3) in series;

the other end of the sixth capacitor (C3) connects with one end of a twentieth resistor (R29) and a first detecting circuit terminal (TX-) in parallel;

the other end of the twentieth resistor (R29) connects with a second power supply (VEE), a collector of the triode (Q1) connects with a second detecting circuit terminal (TX+) and one end of a seventh capacitor (C2) in parallel; and the other end of the seventh capacitor (C2) connects with the first detecting circuit terminal (TX-);

a fourth pin (5) of the auxiliary CPU (MCU2) connects with a clock (OSC), and a fifth pin (1) of the auxiliary CPU (MCU2) connects with ends of a twenty-first resistor (R25) and an eighth capacitor (C5) in parallel;

the other end of the twenty-first resistor (R25) connects with a third power supply (VCC), and the other end of the eighth capacitor (C5) is grounded;

in the auxiliary CPU, a sixth pin (15) connects with a first chip connection (DONE), a seventh pin (16) connects with a second chip connection (CMD0), an eighth pin (17) connects with a third chip connection (CMD1), a ninth pin (18) connects with a fourth chip connection (CMD2), a tenth pin (19) connects with a fifth chip connection (CMD3), and a power supply connection pin (20) connects with the third power supply (VCC) and one end of a ninth capacitor (C19) in parallel; and

the other end of the ninth capacitor (C19) connects with a grounding pin (10) of the auxiliary CPU (MCU2) and the ground in parallel.

5. (Currently Amended) The wireless and passive ~~tablet~~ tableting apparatus of claim 1, wherein the connection relations of said integrating circuit are as follows:

an input terminal (IN) connects with one end of a twenty-second resistor (R21) in series;

the other end of the twenty-second resistor (R21) connects with a negative input pin (2) of a fifth amplifier (IC10A), a first connection pin (11) of an integrating circuit chip (IC8D) and one end of a tenth capacitor (C21) in parallel;

the other end of the tenth capacitor (C21) connects with an output pin (10) of the integrating circuit chip (IC8D) and an output pin (1) of the fifth amplifier (IC10A) in parallel;

a second connection pin (12) of the integrating circuit chip (IC8D) connects with the primary CPU; and

in the fifth amplifier (IC10A), a positive input pin (3) connects with a reference voltage, a grounding pin (4) connects with an analogue ground, a power supply connection pin (8) connects with a power supply (VDD), and the output pin (1) connects with one end of a twenty-third resistor (R20), the other end of the twenty-third resistor (R20) is used as an output terminal and connected with the primary CPU.

6. (Previously Presented) The wireless and passive tableting apparatus of claim 5, wherein, the input terminal of the integrating circuit is connected to an output (OUT) terminal of the phase angle and amplitude detecting circuit, and generates two sets of signals of I phase and J phase having a phase difference of 90 degrees.

7. (Previously Presented) The wireless and passive tableting apparatus of claim 1, wherein, the connection relations of the parallel resonant circuit in the pen circuit are as follows:

an inductor (L1) connects directly with a variable capacitor (C1) and a plurality of capacitors (C2, C3, C4, C5, C6 and C7) in parallel;

the plurality of capacitors connect directly in parallel with a series combination of a switch (K1) and a resistor (R1), wherein one end of the switch (K1) and one end of the resistor (R1) are directly connected, and

the other end of the switch (K1) connects with the other end of the resistor (R1), to form a loop.

8. (Currently Amended) The wireless and passive tableting apparatus of claim 7, wherein, [[a]] the switch (K1) of the pen is a switch on the pen, functioning as the right button of a mouse.